

REMARKS

Applicant thanks the Examiner for indication that claim 1 is drawn to allowable subject matter.

The acceptance of the drawings filed on October 10, 2003 is also noted with appreciation.

The Examiner objected to the abstract as too lengthy. Responding to this objection the abstract was amended to eliminate the unnecessary details, and now comprises less than 150 words.

The specification was carefully checked and in order to more clearly describe the process of formation of recess areas 65 has been amended. Specifically, paragraph two on page 19 was slightly amended to emphasize the moment in the technological process when recess areas are created. Additionally, the typographical error on page 7 has been corrected.

Claim 1 has been objected for the lack of antecedent basis of the limitation "the minimum feature size, F,". Responding to this objection, claim 1 has been amended to substitute for the definite article "the" in front of "minimum feature size, F," with the indefinite article "a".

Claims 1 to 3 are currently pending in the application. By this amendment, claim 1 was amended. Claim 1 was indicated as drawn to the allowable subject matter.

Claims 2-3 have been rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,087,225 to Bronner et al. This rejection is respectfully traversed.

The present invention aims to achieve compatibility between array transistor structures and logic transistors with limited process complexity and high manufacturing yield using a borderless source/drain contact technique. The present invention employs recently developed borderless contacts between the gates. In general, borderless contacts exploit differential etch rate techniques in an area that overlaps two materials (often SiO₂ and SiN) in order to form a sub-lithographic size structure extending orthogonally to the chip surface and allows to form a contact even the distance is short.

The reference to Bronner et al. discloses a method of forming integrated circuit chip with two dissimilar type transistors. The problem resolved by the invention to Bronner et al. resides in a collection of problems which take place on a chip wherein dynamic random access memory and logic designs are combined. It is well known, that a logic design and memory structures

have different properties. For instance, the memory design is focused on minimizing leakage currents which reduce memory cell data retention time when logic structures aims to increase speed at the cost of increased power. In DRAM cells it is necessary to boost the wordline voltage above the circuit power supply voltage to increase the charge stored on storage nodes and to improve resulting signals read therefrom. When wordline voltage is boosted the electric field across the gate dielectric is increased. In order to satisfy gate dielectric reliability, the transfer transistor gate dielectric is thickened. However, the thickened gate oxide degrades performance in peripheral circuits and input/output circuits, affecting general DRAM performance. In the case when memory cells are combined on the chip with logic cells, the logic becomes prohibitively slow. The invention to Bronner et al. in order to improve a performance of the chip with combination of memory and logic cells uses the technique known as dual gate process, wherein two different gate oxide thicknesses on the same chip are provided. The dual gate structure allows improvement of logic performance and increase circuit design flexibility. The process of creating a dual gate oxide is as follows: first, an initial gate oxide is grown and then the gate oxide is photolithographically patterned to protect thick gate oxide region and expose thin oxide gate regions. After that the oxide is etched from the exposed regions. The mask is removed and, oxide is grown in the thin oxide regions and simultaneously thickened in the initially protected gate oxide regions. In short, the patent to Bronner et al. teaches the method of formation of merged DRAM/logic chip with selectively formed dual gate oxide thicknesses.

Paraphrasing the claim 2 of the present invention, the Examiner states in the office action that the reference to Bronner discloses "a borderless source/drain contact (not shown) at a spacer 138 adjacent to said thick cap insulator 110". (page 4 of the Office Action). The Examiner admits that the claimed impurity concentration is not shown by the drawings and there is no description of it in the specification. Additionally, Applicant respectfully points out to the Examiner that the structure defined by the term borderless source/drain contact and its claimed location relative to a thick nitride cap which supports the claimed high impurity concentration is not used by Bronner et al.

Referring to pages 7-8 and 25-26 while one of ordinary skill might be able to theorize that such a high impurity concentration may be desirable, claim 2 and 3 are directed to a combination

of structure which Bronner et al. does not teach which cannot be achieved within the level of ordinary skill in the art discernable from Bronner et al. That is, while a characteristic of a feature might be known to be desirable, a claim to a combination of structures is not *prima facie* shown to be obvious unless the level of ordinary skill in the art would support its achievement.

Additionally, referring to claim 3, the Examiner asserts that Bronner et al. discloses the semiconductor integrated circuit wherein said array transistors are separated by a minimum lithographic feature size for the reason that it is common in the art because a separation of minimum lithographic feature size between array transistors would reduce the size of the device. However, it should be respectfully noted that in order to get the structure of minimum lithographic feature size so-called borderless contacts should be used. According to the present invention borderless technique is used for formation of array transistors whether vertical or planar in view of their close spacing. This technique allows to create sub-lithographic spaces between the transistors in array.

The claim 2 reads, "A semiconductor integrated circuit including array transistors having metal gate conductors encapsulated by a diffusion barrier including a thick cap insulator and a borderless source/drain contact at a spacer adjacent said thick cap insulator, and

logic transistors having silicided contacts, extension implants and a dual work function semiconductor gate having an impurity concentration of greater than 4×10^{20} ." (Emphasis added)

As it can be seen claim 2 contains a limitation about borderless source/drain contact which allows to create really compact structure of array transistors in the present invention. Since the Examiner does not show the fact that the above limitations are not taught or suggested by the reference to Bronner et al., this reference cannot be used to support a *prima facie* obviousness rejection under §103. Based on the above discussion it is respectfully requested that the rejection based on 35 U.S.C. §103 be withdrawn, claims 2 and 3 allowed and application passed to issue.

In view of the foregoing amendments and remarks, Applicant submits that all of the claims are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number

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listed below, if needed. Applicant hereby makes a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0458 (IBM Fishkill).

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'O. Merkoulouva', with a horizontal line extending to the left and a small flourish at the end.

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